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AU Optronics Corporation

Tel: +886-3-563-2899

Fax: +886-3-564-5785

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Product Specification

1.91" COLOR TFT-LCD Semi-Module

MODEL NAME: H191IN02 V0

- () Preliminary Specification
- () Final Specification

Note: The content of this specification is subject to change.

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Record of Revision

Version	Revise Date	Page	Content
0	Dec. 24rd, 2007	20	First draft

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A. General Specification

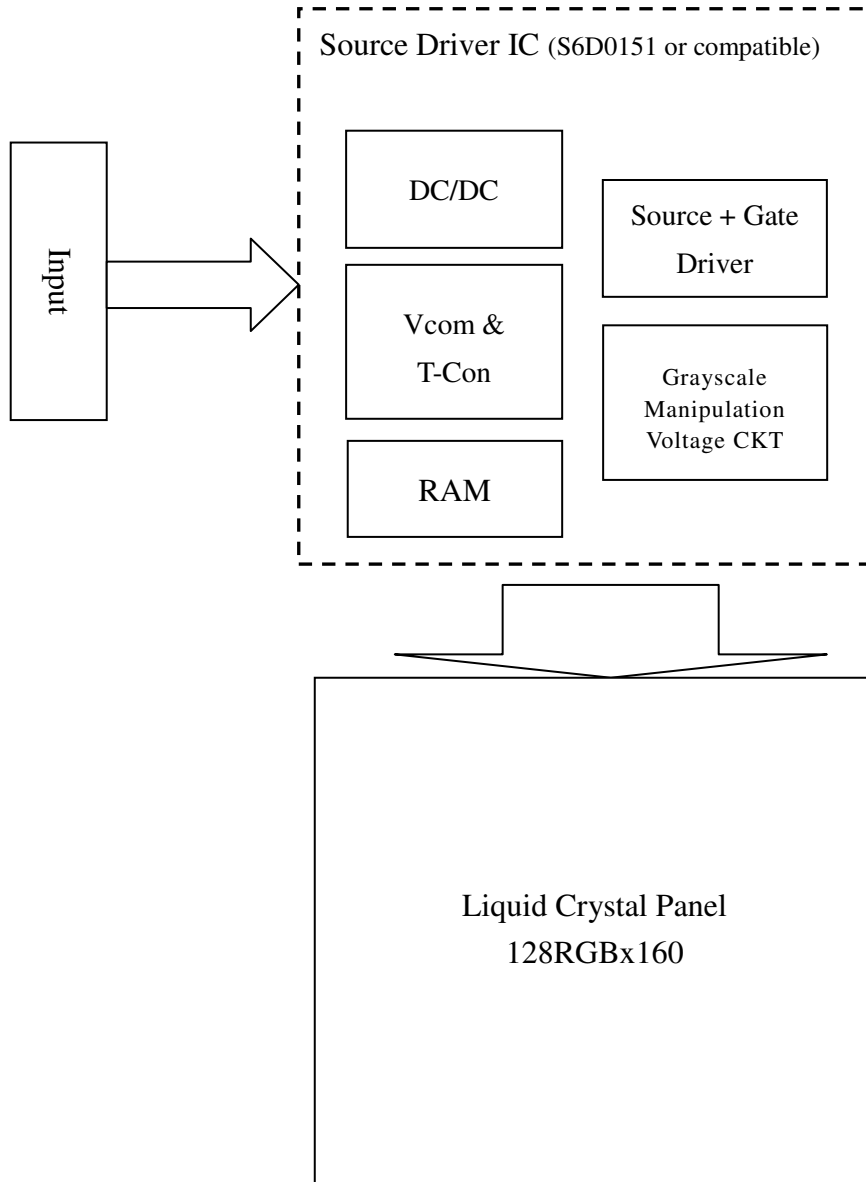
The specification shall be applicable to the TFT-LCD product with polarizer, driver IC which is designed for cellular phones, without FPC, and backlight unit attached. (Except remarked with special description)

1. Physical specifications

NO.	Item	Specification	Remark
1	Display method	Active matrix TFT	
2	Display mode	Transmissive type	
3	Display resolution (dot)	128 X RGB(V) X 160(H)	
4	Active area (mm)	30.34(W) x 37.92(H)	
5	Screen size (inch)	1.91(diagonal)	
6	Pixel pitch (mm)	0.079 x RGB (V) x 0.237(H)	
7	Color configuration	R. G. B. strip	
8	Display color	16/18 bits, 65K /262 K colors	With IC operated
9	Surface treatment	Anti-Glare (Haze 25%)	
10	Overall dimension (mm)	33.736(W) x 45.42(H) x 1.08(D)	Polarizer attached
11	Gray scale inversion	12 o'clock	IC pad on bottom
12	Viewing direction	6 o'clock	
13	Weight (g)	3.5+_0.5	
14	Display viewing area location	Centered	
15	Driver IC type	COG type on glass center	
16	Compatible driver IC of design	Samsung S6D0151	

Remark: All the completed panels were inspected by full function testing after production process were completed. As the electronic/production procedure/testing restrictions, ***“there will never be aging process included within the production process”***.

2. Block diagram



The TFT-LCD module should be completed by preparing polarizer, driver IC.

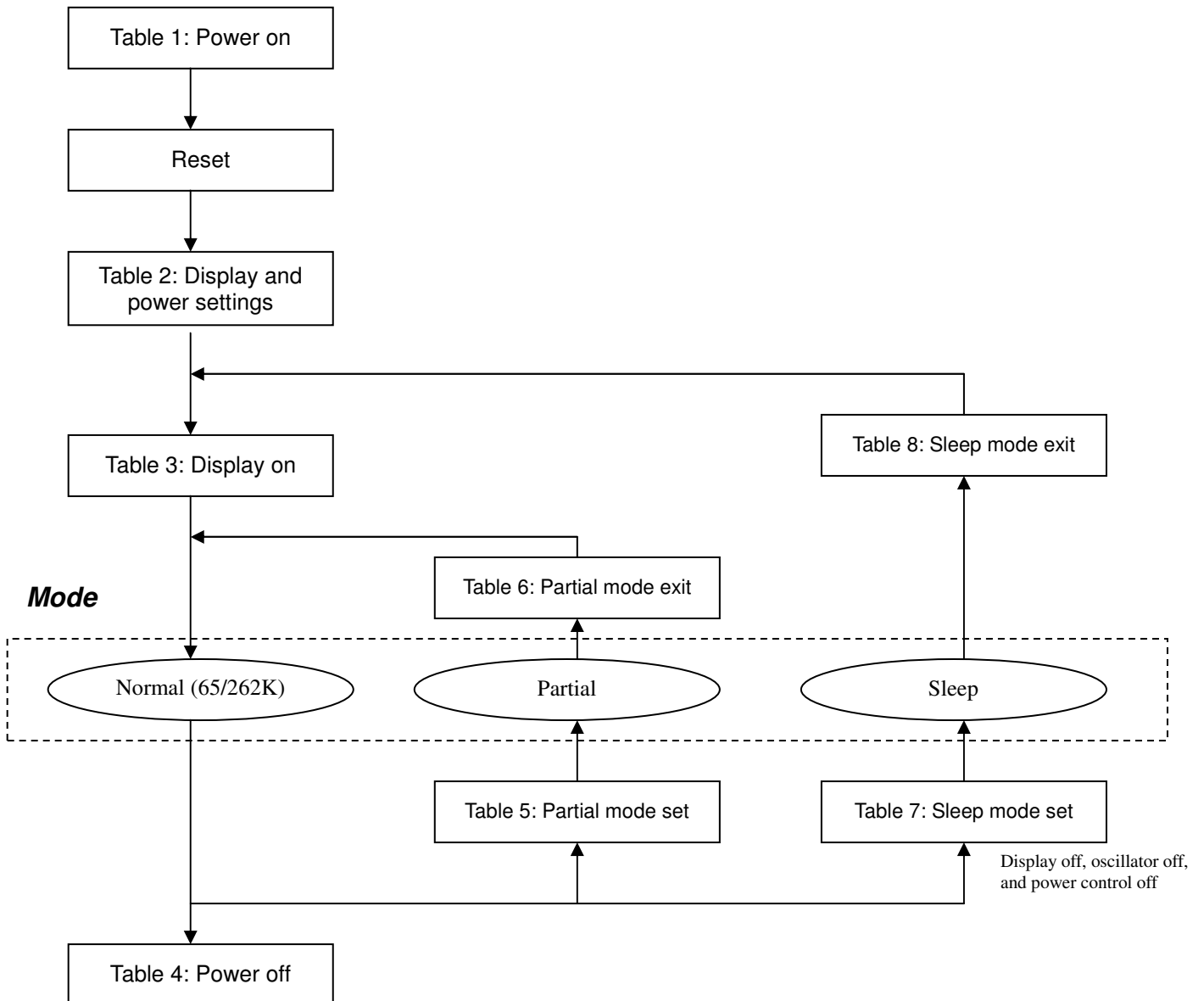
B. Electrical specifications

1. FPC PAD pin assignment *(please refer to the IC specification – Samsung S6D0151)*

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	DUMMY	49	VSS	97	DUMMY
2	DUMMY	50	VGS	98	VGH
3	VCOM	51	CSB	99	VGH
4	VCOM	52	RS	100	VGH
5	VCOM	53	E_WRB	101	VCOMOUT
6	R_OUT	54	PWB_RDB	102	VCOMOUT
7	R_IN	55	ENABLE	103	TG
8	TG	56	DOTCLK	104	R_OUT
9	VCOMOUT	57	HSYNC	105	R_IN
10	VCOMOUT	58	VSYNC	106	VCOM
11	C23+	59	SDI	107	VCOM
12	C23+	60	SDO	108	VCOM
13	C23-	61	DB0	109	DUMMY
14	C23-	62	DB1	110	DUMMY
15	C11+	63	DB2		
16	C11+	64	DB3		
17	C11-	65	DB4		
18	C11-	66	DB5		
19	VCL	67	DB6		
20	VCL	68	DB7		
21	AVDD	69	DB8		
22	AVDD	70	FLM/TEST_OUT		
23	AVDD	71	DB9		
24	GVDD	72	DB10		
25	GVDD	73	DB11		
26	VCOMR	74	DB12		
27	VCOMH	75	DB13		
28	VCOMH	76	DB14		
29	VCOML	77	DB15		
30	VCOML	78	DB16		
31	VCI1	79	DB17		
32	VCI1	80	RESETB		
33	VCI1	81	IM3		
34	VCI	82	IM2		
35	VCI	83	IM1		
36	VCI	84	IM0		
37	VDD3	85	VGL		
38	VDD3	86	VGL		
39	VDD3	87	VGL		
40	RVDD	88	C21-		
41	RVDD	89	C21-		
42	VDD	90	C21+		
43	VDD	91	C21+		
44	VSSA	92	C22-		
45	VSSA	93	C22-		
46	VSSC	94	C22+		
47	VSSC	95	C22+		
48	VSS	96	DUMMY		

2. Operation sequence

- a. Flow chart (by S6D0151) –The registers below are designed for the TFT-LCD based on the driver IC specification of Samsung S6D0151. The panel performance or quality is not guaranteed while the extra testing or design conditions operated not listed in the specification.



b. Command sequence table

Table 1. Power on

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
1	Power On				
Wait 1ms					
H/W Reset					
2	Software Reset Control	0	0	R72h	
		0	1	0x0000	
3	Start Oscillation	0	0	R00h	--Start Oscillation
		0	1	0x0001	
Wait 10ms					

Table 2. Display and power setting

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
1	MTPSEL	0	0	RB4h	--MTPSEL OFF(IF NOT USE MTP)
		0	1	0x0000	
2	Power Control 2	0	0	R12h	--VCI1:2.40V ; first setting Low VCI1 voltage
		0	1	0x0051	
3	Power Control 3	0	0	R13h	--Select VCOMH voltage adjusting
		0	1	0x0800	--First setting operation amplifier OFF
4	Power Control 4	0	0	R14h	--Setting VCOML voltage level negative voltage
		0	1	0x72EC	--Setting COM output amplifier voltage: 5.1612V(GVDD*1.122) --Setting VCOMH level voltage:4.5793V(GVDD*0.9955)
5	Setting internal oscillator oscillation frequency	0	0	R61h	--Setting internal OSC Freq. :275.52K(Follow customer rule to frame Freq. :105Hz)
		0	1	0x001B	
6	Power Control 1	0	0	R10h	--Source OP level 04.
		0	1	0x240C	--VGH voltage:13.2V (AVDD*2+VCI1) --VGL voltage :-10.56V -(AVDD*2)
Wait 80ms					

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
7	Power Control 3	0	0	R13h	--Select VCOMH voltage adjusting
		0	1	0x0810	--setting operation amplifier ON --Setting GVDD=4.60V
Wait 20ms					
8	Power Control 2	0	0	R12h	-- Setting VCI1 voltage : 2.64V
		0	1	0x0092	--Setting GVDD=4.60V
9	Driver output Control	0	0	R01h	--SS="H" --GS="L"
		0	1	0x0114	--SM="H" --NL[4:0]="10100";Drive line
10	LCD Driver waveform control	0	0	R02h	--FL[1:0]="01"
		0	1	0x0100	--FLD="L"
11	Entry mode	0	0	R03h	--BGR="L" --MDT[1:0]="00"
		0	1	0x1030	--ID[1:0]="11" --AM="L"
12	Blank Period Control	0	0	R08h	--FB[3:0]="0010", 2 line
		0	1	0x0202	--BP[3:0]="0010", 2 line
13	Frame cycle Control	0	0	R0Bh	--DIV[1:0]="00", Division Ratio:1
		0	1	0x0000	--RTN[3:0]="0000", 16(INCLKs) * IF Frame Freq.=105Hz
14	External Interface Control	0	0	R0Ch	--RM="L"
		0	1	0x0000	--DM[1:0]="00" --RIM[1:0]="00"
15	Setting internal oscillator oscillation frequency	0	0	R61h	--Setting internal OSC
		0	1	0x001B	Freq. :275.52K(Follow customer rule to frame Freq. :105Hz)
16	Low Power mode	0	0	R69h	--NLPM="0" ,Normal
		0	1	0x0000	--NLDC[3:0]="0000"
17	source output pre-driving period	0	0	R70h	--EQ[1:0]="11",EQ=3
		0	1	0x0003	--SDT[1:0]="00"
18	Gate output period Control	0	0	R71h	--GNO[1:0]="00"
		0	1	0x0000	

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
19	Gamma Control 1	0	0	R11h	--Gamma setting
		0	1	0x0004	
20	Gamma Control 2	0	0	R30h	--Gamma setting
		0	1	0x0000	
21	Gamma Control 2	0	0	R31h	--Gamma setting
		0	1	0x0207	
22	Gamma Control 2	0	0	R32h	--Gamma setting
		0	1	0x0101	
23	Gamma Control 2	0	0	R33h	--Gamma setting
		0	1	0x0000	
24	Gamma Control 2	0	0	R34h	--Gamma setting
		0	1	0x0504	
25	Gamma Control 2	0	0	R35h	--Gamma setting
		0	1	0x0002	
26	Gamma Control 2	0	0	R36h	--Gamma setting
		0	1	0x0706	
27	Gamma Control 2	0	0	R37h	--Gamma setting
		0	1	0x0200	
28	Gamma Control 3	0	0	R38h	--Gamma setting
		0	1	0x0400	
29	Gate Scan Position	0	0	R40h	--SCN[4:0]="00000"
		0	1	0x0000	
30	1'st screen driving Position	0	0	R42h	--SE1=159 --SS1=0
		0	1	0x9F00	
31	2'nd screen driving Position	0	0	R43h	--SE2=0 --SS2=0
		0	1	0x0000	

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
32	Horizontal window address	0	0	R44h	--HEA=127
		0	1	0x7F00	--HAS=00
33	Vertical window address	0	0	R45h	--VEA=159
		0	1	0x9F00	--VSA=0
34	GVDD bias control register.	0	0	RBFh	-- IVRH_3-0 : GVDD bias current control. (min=RBFh b0000 ~ max b1111h) -- Default = 0x0000
		0	1	0x1000	
Display ON Sequence					
35	RAM address	0	0	R21h	--AD15 - AD0 address
		0	1	address	
36	Write data to GRAM	0	0	R22h	--RD15 – RD0
		0	1	Data	

Table 3. Display on

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
1	Display Control	0	0	R07h	--GON=0,DTE=0,D[1:0]="01" --REV=1
		0	1	0x0005	
Wait more than 1ms					
2	Display Control	0	0	R07h	--GON=1,DTE=0,D[1:0]="01" --REV=1
		0	1	0x0025	
3	Display Control	0	0	R07h	--GON=1,DTE=0,D[1:0]="11" --REV=1
		0	1	0x0027	
Wait more than 2 frame					
4	Power Control 4	0	0	R07h	--DTE=1,GON=1,DTE=0,D[1:0]="11" --REV=1
		0	1	0x0037	

Table 4. Display off

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
1	Display Control	0	0	R07h	--GON=1,DTE=1,D[1:0]="10"
		0	1	0x0032	
Wait more than 2 frame					
2	Display Control	0	0	R07h	--GON=1,DTE=0,D[1:0]="10"
		0	1	0x0022	
Wait more than 1ms					
3	Display Control	0	0	R07h	--GON=1,DTE=0,D[1:0]="00"
		0	1	0x0027	
Wait more than 2 frame					
4	Power Control 3	0	0	R13h	--PON=0
		0	1	0x0000	
5	Power Control 1	0	0	R10h	--SAP=0,AP=0
		0	1	0x0000	
Display OFF					

Table 5. Standby mode on

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
Display OFF Sequence					
1	Power Control 1	0	0	R10h	--STB ON
		0	1	0x0002	

Table 6. Standby mode off

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
1	Start Oscillation	0	0	R00h	--OSC ON
		0	1	0x0001	
Wait 10ms					
2	Power Control 1	0	0	R10h	--STB off
		0	1	0x1C0C	
3	Software Reset Control	0	0	R72h	--Software reset
		0	1	0x0000	
4	Display and power setting sequence				

Table 7. Sleep mode on

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
Display OFF Sequence					
1	Start Oscillation	0	0	R10h	--SLP on
		0	1	0x0002	

Table 8. Sleep mode off

INSTRUCTION		R/W	D/C	REG	DESCRIPTION
1	Power Control 1	0	0	R10h	--SLP off
		0	1	0x1C0C	
2	Software Reset Control	0	0	R72h	--Software reset
		0	1	0x0000	
4	Display and power setting sequence				

3. Absolute maximum ratings ($V_{SS}=0V$) (Note 1)

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Logic supply voltage	VDD		-0.3	3.3	V	
Supply voltage for step-up circuit	VCI		-0.3	4.0	V	
LCD supply voltage range	VGH-VGL		-	30	V	
Operating temperature	Topa		-30	70	°C	
Storage temperature	Tstg		-40	85	°C	
Storage humidity	Hstg		10	90	%	

Note 1: If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop. It is not allowed for any of these ratings to be exceeded. Make sure all the design characteristics are adequate before the panel is initialed.

Note 2: All the measurements should be operated with driver IC and experimental FPC mounted.

4. Electrical characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Input power supply	VDD3	1.7	1.8	3.0	V	Note 1
	VCI	2.7	2.8	3.0	V	
Input Signal Voltage	H Level	V_{IH}	$0.8 \times VDD3$	-	VDD3	V
	L Level	V_{IL}	0	-	$0.2 \times VDD3$	V
Output signal voltage	H Level	V_{OH}	$0.7 \times VDD3$	-	VDD3	V
	L Level	V_{OL}	0	-	$0.3 \times VDD3$	V

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during operation. To prevent noise, a bypass capacitor must be inserted into the line close to power pin. Please make sure all the design settings are used within this range before the panel is initialed.

Note 2. Please make sure that DC is not supplied to LCD for long period. And do not supply voltage to LCD while within "sleep mode".

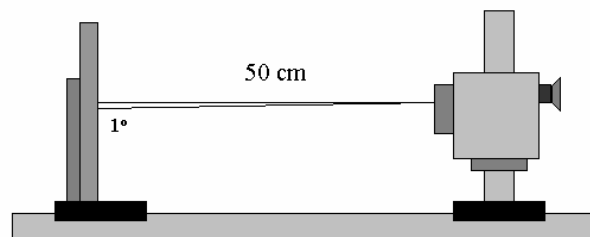
C. Optical specification (Note 1, Note 2, Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time (with polarizer)	Rise	Tr	$\theta=0^\circ$	-	12	20	ms	Response time (with polarizer)
	Fall	Tf		-	18	30	ms	
Contrast ratio (with polarizer)		CR	At optimized Viewing angle	200	250	-		Note 5, 6
Viewing angle (with polarizer)	Top		$CR \geq 10$	40	60	-	degree	Viewing angle (with polarizer)
	Bottom			10	15	-		
	Left			25	40	-		
	Right			25	40	-		
Transmittance (with polarizer)				6.8	7.3			
Color filter coordination		Rx	$\theta=0^\circ$		0.58			simulated by LED light source, which is provided by customer
		Ry			0.34			
		Gx			0.32			
		Gy			0.58			
		Bx			0.15			
		By			0.11			
		Wx			0.30			
		Wy			0.32			

Note 1: Ambient temperature = $25^\circ\text{C} \pm 2^\circ\text{C}$. Tested with driver IC and experimental FPC attached.

Note 2: To be measured in the dark room.

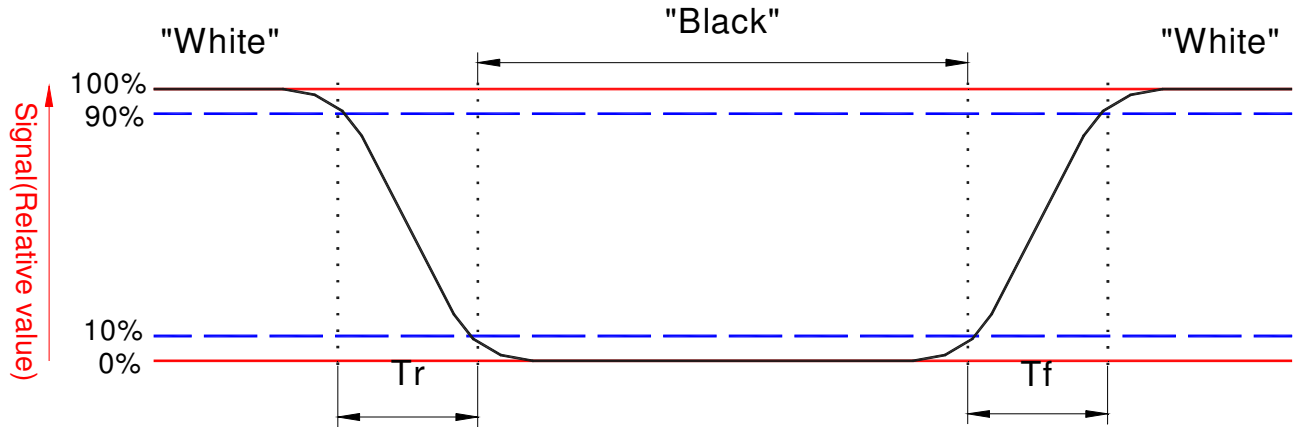
Note 3: To be measured at the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7, after 10 minutes operation (module).



Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below:



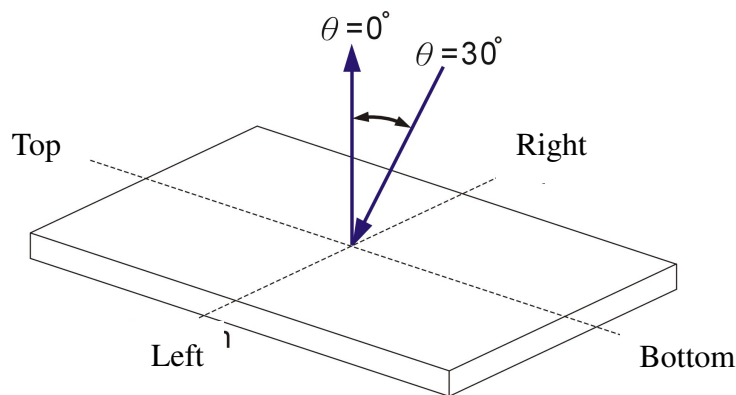
Note 5. White $V_i=0.9V$
 Black $V_i=4.5V$

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6. Definition of contrast ratio:
 Contrast ratio is calculated with the following formula.

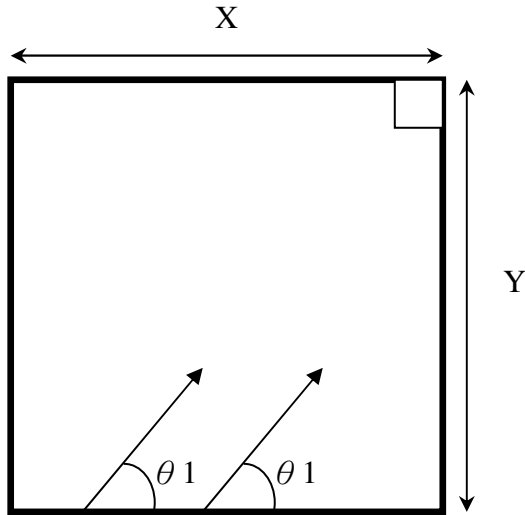
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 7. Definition of viewing angle:
 Refer to the figure as below.



D. Absorption angle of display

Absorption axis θ is the angle of the light absorption direction when see it from the **protect film** side of the polarizer.



Polarizer Model	Dimension (mm)		Absorption Angle (θ)
	X	Y	
By customer design features	By customer LCM design features		45 degree

E. Reliability test items

The panel performance shall meet the judgment criteria after the testing items have been performed. However, only a single item of these tests shall be executed on a single panel. No more one test item shall be executed on a single panel.

1. Test items and conditions (Note 1)

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240H	
2	Low temperature storage	Ta= -30℃ 240H	
3	High temperature operation	Ta= 70℃ 240H	Operation
4	Low temperature operation	Ta= -20℃ 240H	Operation
5	High temperature and high humidity	Ta= 60℃ . 90% RH 240H	Operation
6	Thermal shock Test	Cycle display from -40℃ to +85℃ with 5-minute transfer time. 15 minute dwell, 15 cycles	Non-operation
7	Vibration Test	Amplitude: 20mm 5Hz, 1G/45 min for each X,Y,Z	Non-operation Package
8	Drop Test (package state)	Height: 60cm 1 corner, 3 edges, 6 surfaces	Each direction 1 time

Ta: Ambient temperature.

Note 1: All the tests are performed by whole set of TFT-LCD module with completed driver IC, FPC, and backlight module.

2. Failure Judgment Criteria

- a. After the test, the panel should be left at room temperature and room humidity (15℃~35℃, 45%~65% RH). Then the panel could be inspected for normal operation.
- b. Neither abnormality nor significant visible deterioration should be found on display performance.
- c. There should be no functions abnormalities on display quality.

F. Mechanical specifications

